WHAT IS CLAIMED IS:

1. A method of manufacturing a capacitor of a semiconductor device, the method comprising the steps of:

i) sequentially depositing a first insulating layer, an etching stop layer, and a second insulating layer on a semiconductor substrate;

ii) etching a predetermined portion of the second insulating layer to form a preliminary hole for exposing the etching stop layer;

iii) forming a first hole by transversely expanding the preliminary hole in the second insulating layer;

iv) forming a second hole by etching a predetermined portion of the etching stop layer and the first insulating layer at a bottom surface of the first hole, the second hole making contact with an electrode area of the semiconductor substrate and having an area narrower than the first hole;

v) forming a first conductive layer pattern uniformly on sidewalls of the first and second holes and on a bottom surface of the second hole; and

vi) sequentially depositing a dielectric layer and a second conductive layer pattern on the first conductive layer pattern.

2. The method as claimed in claim 1, wherein the steps of forming the first and the second holes comprise the substeps of:

a) providing a photoresist pattern for forming the preliminary hole on the second insulating layer;

b) anisotropically etching the second insulating layer using the photoresist pattern as an etching mask to form the preliminary hole and exposing the etching stop layer;

c) isotropically etching a sidewall of the preliminary hole in the second insulating layer to transversely expand the preliminary hold to form the first hole; and

d) anisotropically etching a predetermined portion of the exposed etching stop layer and the first insulating layer at the bottom surface of the first hole using the photo-resist pattern as the mask to form the second hole and expose the semiconductor substrate.

3. The method as claimed in claim 2, wherein a hole in the photo-resist pattern is formed on a portion of the second insulating layer in an area that corresponds to an upper center portion of the electrode area of the semiconductor substrate.

4. The method as claimed in claim 2, wherein the first and second insulating layers are etched at an etching selectivity ratio of 5-25 to 1 with respect to the photoresist pattern.

5. The method as claimed in claim 2, wherein the anisotropic etching with respect to the first and second insulating layers is carried out by a dry etching process by supplying a mixed gas including C_5F_8, O_2, CH_2F_2, Ar, and CO at an appropriate combination of the gas components.

6. The method as claimed in claim 2, wherein the isotropic etching with respect to the sidewall of the preliminary hole is carried out such that the second insulating layer has an etching selectivity ratio of about 10-40 to 1 with respect to the etching stop layer.

7. The method as claimed in claim 2, wherein the isotropic etching with respect to the sidewall of the preliminary hole in the second insulating layer is carried out by a wet etching process.

8. The method as claimed in claim 1, wherein the first and second insulating layers are formed to a thickness in a range between about 100 and about 1500 nm using materials having insulating and reflowing characteristics,.

9. The method as claimed in claim 1, wherein the etching stop layer is formed by depositing a silicon nitride or a silicon oxy-nitride material.

10. The method as claimed in claim 1, wherein the etching stop layer has a thickness in a range between about 5 and about 200 nm.

11. The method as claimed in claim 1, wherein the step of forming the first conductive layer pattern comprises the substeps of:

a) depositing a first conductive layer on the sidewalls of the first and second holes, on the bottom surface of the second hole, and on the second insulating layer; and

b) etching back the first conductive layer until the second insulating layer outside the first and second hole is exposed.

12. The method as claimed in claim 11, wherein the first conductive layer has a thickness in a range between about 20 to about 200 nm.

13. The method as claimed in claim 11, wherein the etch-back step is carried out by a dry etching process or a chemical mechanical polishing process.

14. The method as claimed in claim 11, further comprising the step of depositing a hemispherical silicon grain (HSG) layer on the first conductive layer pattern which is deposited on the sidewalls of the first and second holes and on the bottom surface of the second hole.

15. The method as claimed in claim 1, wherein after forming the first conductive layer pattern, the second insulating layer is removed by a selective etching process to expose both sides of the first conductive layer pattern above the etching stop layer before depositing the dielectric layer and the second conductive layer pattern.

16. The method as claimed in claim 15, further comprising the step of forming a hemispherical silicon grain (HSG) layer on an entire surface of the first conductive layer pattern.

17. The method as claimed in claim 7, wherein the wet etchant is a buffered oxide etchant (BOE).

18. The method as claimed in claim 8, wherein the materials used for forming the first and second insulating layers are boro-phospho-silicate-glass (BPSG) or undoped silicate-glass (USG).

19. The method as claimed in claim 11, wherein the first conductive layer material is doped poly-silicon.

20. The method as claimed in claim 15, wherein the selective etching process is a wet etching process.

21. The method as claimed in claim 11, wherein the etch-back process is performed by a chemical mechanical polishing (CMP) process or a dry etching process.